



Efinix FPGA Security Features

Maximilian Werner, EMEA FAE

V: 1.0

Agenda

- Efinix Introduction
- FPGA Families
- Security features
- IP
- Eval Boards
- Software

Efinix Global

Founded in 2012

Worldwide Presence with 170+ Employees

EMEA HQ: Munich/Unterschleißheim

AE Office: Manchester



Executive Leadership

Ming Ng
COO



Sammy Cheung
Chairman,
President and CEO



Tony Ngai
CTO and
Sr. VP Engineering



Jeff Suto
General Counsel



Harald Werner
Managing Director
(EMEA)



Ikuo Nakanishi
VP Sales and BDM
(JAPI)



Greg Barrett
CFO, Sr. VP Finance



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Engineering



Mark Oliver
VP, Marketing

Distribution Network Europe :

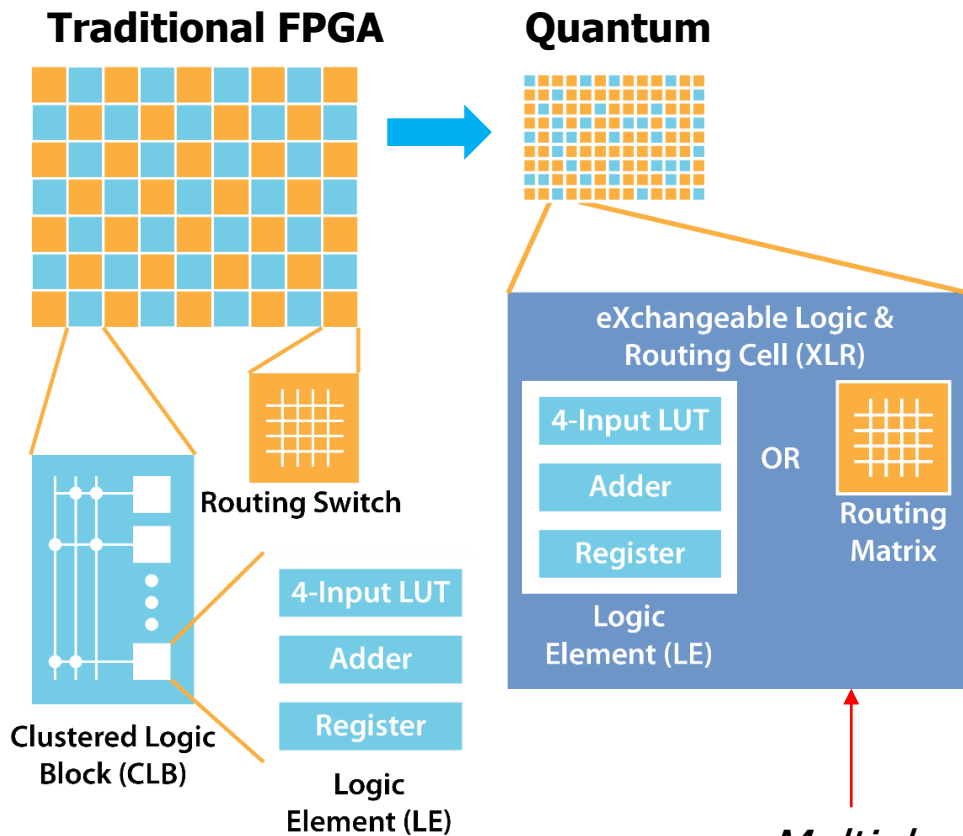
DigiKey



RUTRONIK
ELECTRONICS WORLDWIDE



Quantum FPGA Technology



Advantages over traditional FPGAs

- 4X Better Power-Performance-Area (PPA)
- 7 layers of metal vs. 12+ layers in traditional FPGA
- Single architecture scalable to 1 million+ logic elements (LE)
- Silicon process agnostic

Architectural Highlights

- Flexible, fine grained
- Software configurable logic/routing
- High performance adaptive interconnect
- Hybrid place and route algorithm
- Standard silicon recipe

Trion® FPGAs (Gen 1)

- Focus on **Consumer, Industrial Markets, Communications Markets** with varied applications
 - Traditional FPGA markets
 - Emerging edge AI computing markets
 - Applications: mobile, IoT, LED, automation, robotics, video, audio, sensing integration, display, computer vision, etc.
- 4K to 120K LEs on 40LL SMIC silicon process
- Traditional SRAM-based FPGA
 - Masked option for T20/T13/T8/T4 – boots internally vs. using a configuration device
- Optimized for low power
- Hard core blocks for DDR memory controllers and D-PHY v1.1 and CSI-2 v1.3
 - Up to 3 independent RX/TX interfaces, 4 lanes x 1.5 Gbps



Artificial intelligence (AI) and machine learning algorithms are everywhere, enabling new advances in areas like image and speech recognition and autonomous driving. But applications on the leading edge need a platform that can change as rapidly as they do.

Efinix® Trion™ FPGAs are flexible, programmable platforms that can accelerate AI applications that rely on changing algorithms. Bring your Trion-accelerated product to market quickly today, and change it tomorrow to meet the next challenge.

See how Trion FPGAs are driving edge AI computing!

www.efinixinc.com/drivingai



Trion Family Table

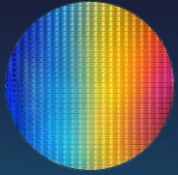
Feature	T4	T8	T13	T20	T35	T55	T85	T120
Logic Elements (LEs)	3,888	7,384	12,828	19,728	31,680	54,195	84,096	112,128
Mask Programmable Memory	√	√	√	√	—	—	—	—
Embedded RAM bits (kb)	77	77	727	1,044	1,475	2,765	4,055	5,407
18 x 18 Multipliers	4	4	24	36	120	150	240	320
49-ball FBGA (0.4 mm, 3x3 mm)	4	33 1 -						
80-ball WLCSP (0.4, 4.5x3.6mm)				33 5 - 1,1 -				
81-ball FBGA (0.5, 5x5 mm)	55 1	55 1 -						
100-pin LQFP (0.5, 14x14 mm)			65 4 4,4 - -	65 4 4,4 - -				
144-pin LQFP (0.5, 20x20 mm)		97 5 6, 6		97 5 6, 6 - -				
169-ball FBGA (0.65, 9x9 mm)			73 5 8,12 2,2 -	73 5 8,12 2,2 -				
256-ball FBGA (0.8, 13x13 mm)			195 5 13,13 - -	195 5 13,13 - -				
324-ball FBGA (0.65, 12x12 mm)				130 7 20,26 2,2 x8,x16	130 7 20,26 2,2 x8,x16	130 7 20,26 2,2 x8,x16	130 7 20,26 2,2 x8,x16	130 7 20,26 2,2 x8,x16
400-ball FBGA (0.8 16x16 mm)				230 7 20,26 - x8,x16	230 7 20,26 - x8,x16			
484-ball FBGA (0.8, 18x18 mm)						256 8 40,40 - x16,x32	256 8 40,40 - x16,x32	256 8 40,40 - x16,x32
576-ball FBGA (0.65, 16x16 mm)						278 8 52,52 3,3 x16,x32	278 8 52,52 3,3 x16,x32	278 8 52,52 3,3 x16,x32

GPIO	PLLs	LVDS Pairs (TX, RX)	MIPI 4-Lane D-PHY with CSI-2 Controller (TX, RX)	DDR3, LPDDR3, LPDDR2 (800 Mbps)
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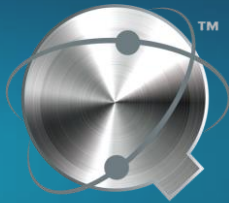
Titanium Under the Hood

- TSMC 16nm Process
 - High Performance for the Most Demanding Applications
 - High Density and Low Power Consumption
- 2nd Generation Quantum Fabric
 - Optimized for Compute & Artificial Intelligence
- High Speed Interfaces
 - Designed for Video and Quantum Acceleration

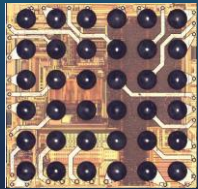




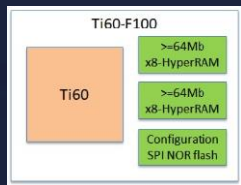
TSMC 16 nm Process



QUANTUM
Quantum Compute
Accelerated



Innovative
Package Options



System in Package

High-Performance Titanium

	Ti35	Ti60	Ti90	Ti120	Ti180	Ti240	Ti375	Ti550	Ti750	Ti1000
LE (k)	36	62	92	123	176	237	370	533	727	969
10K RAM (Mb)	1.53	2.62	7.34	9.80	13.11	19.37	27.53	39.65	54.07	72.09
DSP	93	160	359	478	640	946	1344	1936	2640	3520
PLLs	4	4	10	10	10	10	10	10	10	10
MIPI DPHY 1.5G, support CSI-2/DSI	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
MIPI DPHY x4 2.5Gbps Hard IP	-	-	X4	X4	X4	X3	X3	X3	X3	X3
LPDDR4/X (> 3Gbps)	-	-	X32	X32	X32	2 X32	2 X32	2x72	2x72	2x72
RISC-V hardwired						x	x	x	x	x
16 Gbps Serdes	-	-	X8	X8	X8	X16	X16	X16	X16	X16
25.8 Gbps Serdes	-	-	-	-	-	-	-	X8	X8	X8
PCIe Gen4 (16G) hard controller	-	-	1x PCIe Gen4x4	1x PCIe Gen4x4	1x PCIe Gen4x4	2x PCIe Gen4x4	2x PCIe Gen4x4	2x PCIe Gen4x8	2x PCIe Gen4x8	2x PCIe Gen4x8
Packages (HSIO/HVIO/LPDDR4/MIPI /SERDES)										
W64	0.4mm	3.5x3.4mm	-	34/0			-	-	-	-
F100 (SIP)	0.5mm	5.5x5.5mm	61/0	61/0			-	-	-	-
F225	0.65mm	10x10mm	140/23	140/23			-	-	-	-
J361	0.65mm	13x13mm	-	-	110/20/16/2/0	110/20/16/2/0	110/20/16/2/0	-	-	-
G400	0.8mm	16x16mm			200/74/0/0/0	200/74/0/0/0	200/74/0/0/0			
L484	0.8mm	18x18mm	-	-	116/27/0/4/0	116/27/0/4/0	116/27/0/4/0	-	-	-
J484	0.8mm	18x18mm	-	-	116/27/32/4/0	116/27/32/4/0	116/27/32/4/0	-	-	-
G529	0.8mm	19x19mm	-	-	210/48/32/0/0	210/48/32/0/0	210/48/32/0/0	-	-	-
N529	0.8mm	19x19mm	-	-	-	-	-	100/51/32/0/0	100/51/32/0/0	
N529**	0.8mm	19x19mm	-	-	-	-	-	100/51/32/0/8	100/51/32/0/8	
N676**	0.65mm	18x18mm	-	-	-	-	-	130/60/32/2/12	130/60/32/2/12	
N900**	0.8mm	25x25mm	-	-	-	-	-	172/87/32x2/1/16	172/87/32x2/1/16	
P1156**	1.0mm	35x35mm	-	-	-	-	-	256/118/32x2/3/16	256/118/32x2/3/16	

** subject to change

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F100 (SIP) :16 MbFlash + 256Mbit HyperRAM



Security features

Trion

- You can use MPM method to deploy your bitstream directly to the T4 up to T20 Silicon, where you can select that readout is not possible.
- Only applicable for high volume application as we have to do a new mask, which includes as well NRE cost.
- Not more security features available in Trion.

Titanium Security

Secure Configuration with Trusted Image

- Authentication
 - Public Key Encryption of Signed Digital Bitstream
 - Only Trusted Images Are Loaded Into Device

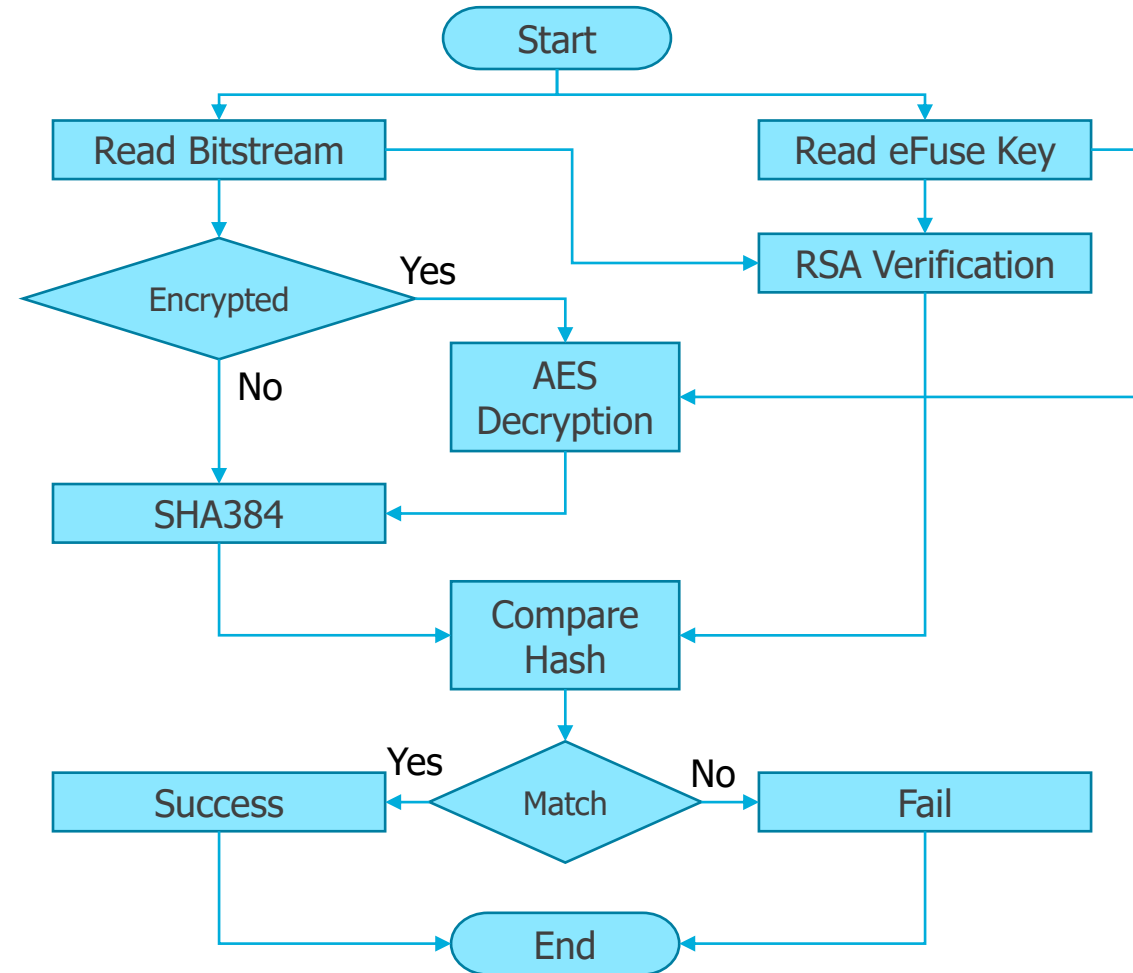
Intellectual Property Protection

- Encryption
 - Configuration Bitstreams Are Encrypted for Copy Protection






Secure Configuration Flow

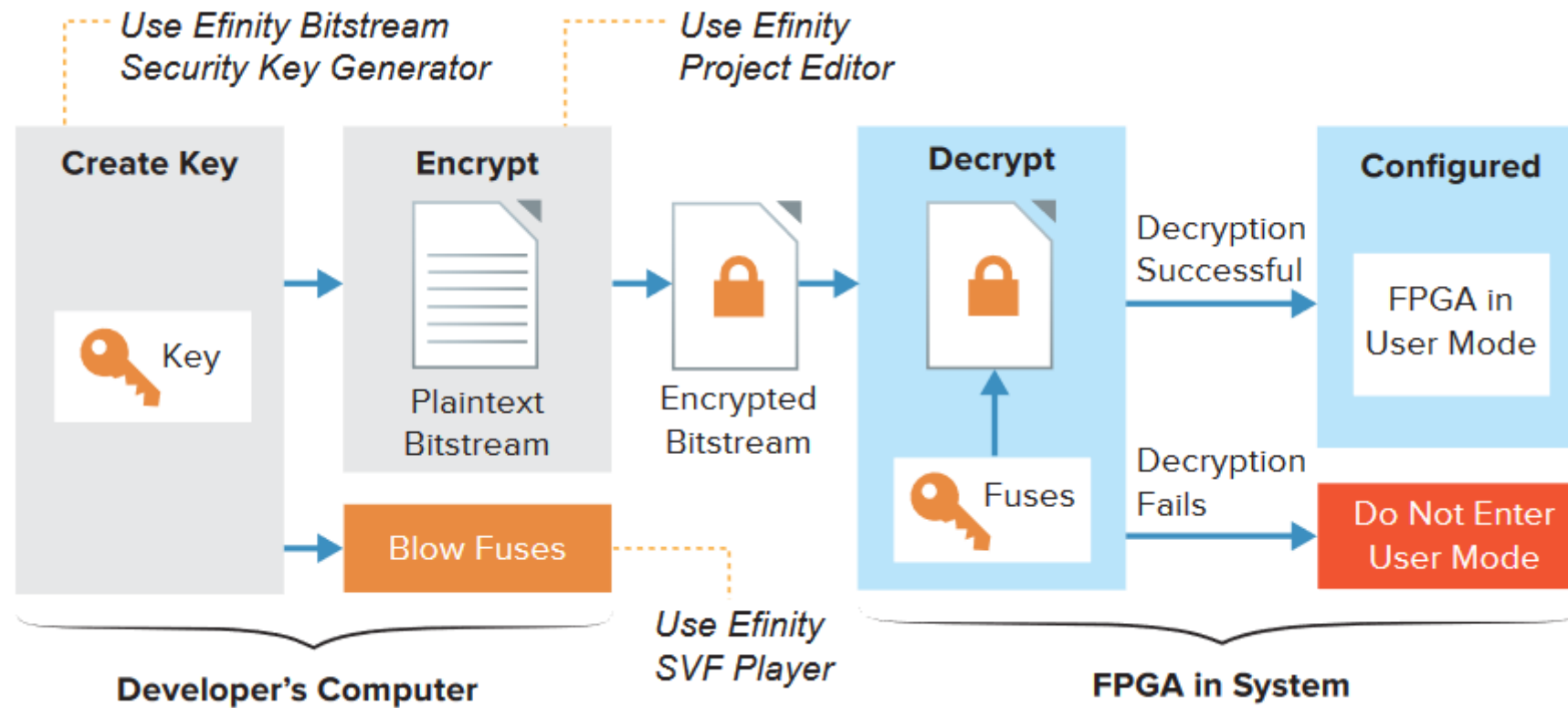
- Public Key RSA4096 Authentication
 - Private Keys Remain With OEM
 - Only Know Good Bitstreams Used
- Private Key AES256 Encryption
 - Lightning-Fast Boot
 - Encryption of Valuable IP
- Totally Secure Root of Trust
 - No Users Access to Security Engine
- eFuse Key Storage
 - OEMs Can Program Their Own Keys During Manufacture
 - Keys Remain Secure Inside Device



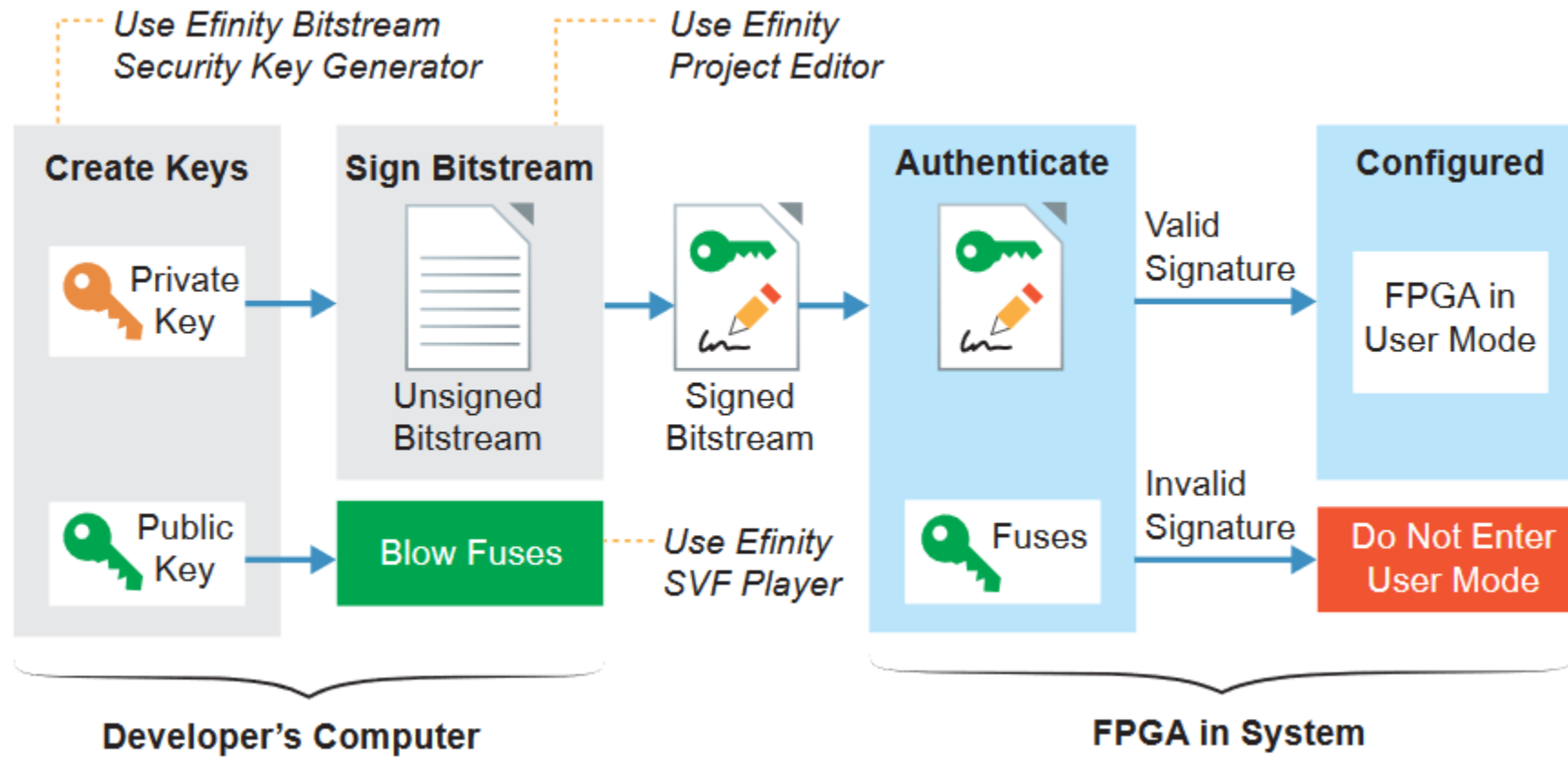
Efinity Tools used for Securing Bitstream

Tool	Used for
 Bitstream Security Key Generator	<p>Create or specify an AES-256 key.</p> <p>Create or specify an RSA-4096 private key.</p> <p>Specify whether to disable JTAG.</p>
 SVF Player	<p>Program the fuses in the Titanium FPGA with the AES-256 key and/or RSA certificate data.</p> <p>After you blow the fuses with an RSA key, the FPGA only accepts a bistream signed with the correct private key.</p> <p>After you blow fuses with an AES-256 key, the FPGA only accepts a plaintext bitstream or a bitstream signed with the correct key.</p> <p>Program the JTAG fuse to disable JTAG function.</p> <p>After you blow the JTAG fuse, you cannot use any JTAG command except IDCODE, DEVICE_STATUS, and BYPASS.</p>
 Project Editor	<p>Turn on bitstream encryption and/or authentication, and specify the .bin file created by the Bitstream Security Key Generator.</p> <p>Turn on bitstream authentication and specify the private key (.pem) file to sign the bitstream.</p>

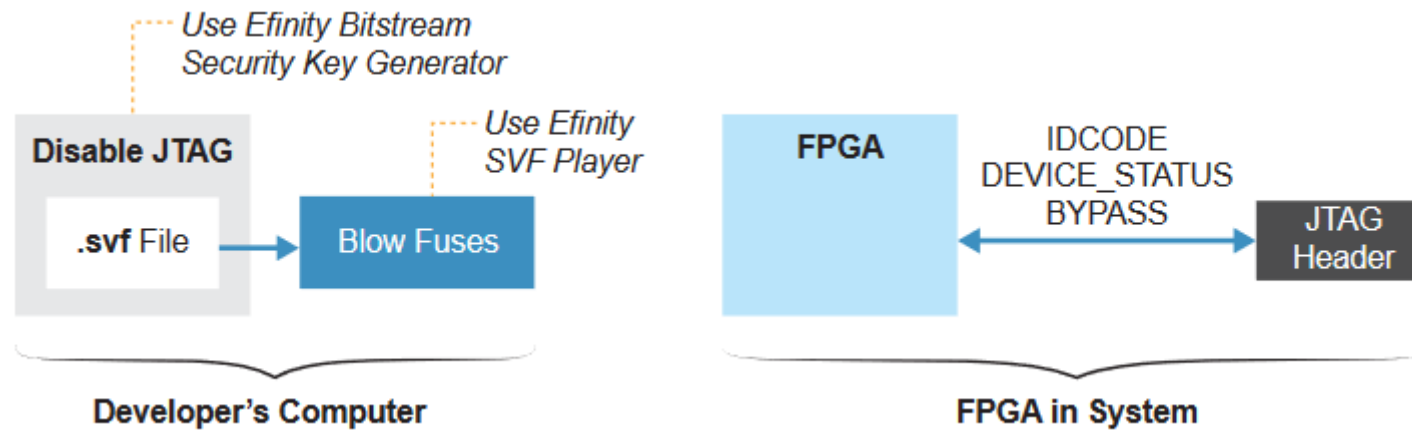
Bitstream Encryption



Bitstream Authentication



Disabling JTAG



Security Key Generator

The screenshot shows the Efinity Bitstream Security Key Generator application window. The interface includes several sections: AES-256 Bitstream Encryption, RSA-4096 Asymmetric Bitstream Authentication, JTAG, and Misc. The AES-256 section has a checked checkbox and a text field containing a 256-bit key. The RSA-4096 section has a checked checkbox and a text field for an RSA PEM file. The JTAG section has a dropdown menu for JTAG Disabling set to OFF. The Misc section has a dropdown menu for Device set to Ti60. A Generate button is located at the bottom right of the main form. A status message box at the bottom displays the output of the generation process.

Annotations on the left side:

- Turn JTAG disabling on or off
- Choose the FPGA

Annotations on the right side:

- If you have your own 256-bit key, enter it here
- Randomly Generate button
Click to generate a new key
- Randomly Generate PEM File button
Click to generate a new key
- Select PEM File
If you already generated an RSA private key, click to choose it
- Click to generate key files and a file for use with the SVF Player
- Status messages

Status messages:

```
Fri October 22 21 14:24:24 - Successfully generate PEM  
File: D:/ti60f100_security_demo/demo/  
demo_10222021.pem
```

Project Editor

Project Design Synthesis Place and Route **Bitstream Generation** Debugger

Active Passive

Active

Clock Source: Internal Oscillator

SPI Programming Clock Divider: DIV8

Clock Sampling Edge: Rising

Power Down Flash After Programming

Use 4-Byte Addressing During Configuration

Programming Mode: SPI active x1

Enable Initialized Memory in User RAMs: on

Release Tri-States Before Reset

Enable Bitstream Compression

Remarks: Compression must be disabled when security feature is enabled

Bitstream Security

Bitstream Encryption

Randomize IV value during compilation

96-bit IV Value:

Bitstream Authentication

FPGA Key Data File:

Cert. File:

Output

Generate JTAG Configuration File

Generate JTAG Raw Binary Configuration File

Generate SPI Configuration File

Generate SPI Raw Binary Configuration File

OK Cancel

Efinity SVF Player

The screenshot shows the Efinity SVF Player application window. The interface includes a menu bar (File, Help), a Target selection dropdown (USB Target: TI60 F225 Development Board), USB Info (ID: 0403:6010 S/N FT5M8ZDJ), and an SVF File path (D:/ti60f225_demo/ti60f225_security_feature.svf). A central console displays the contents of the .svf file, which includes commands like TRST OFF, ENDIR IDLE, STATE RESET, and various TDR, HDR, and SDR commands. At the bottom, there are control buttons for Play, Step, and Stop, and a status message area showing execution progress and completion.

Annotations with dashed orange lines point to specific features:

- Click to refresh the search for a connected board (points to the refresh icon next to the USB Target dropdown)
- Click to refresh the .svf file (points to the refresh icon next to the SVF File text box)
- Load an .svf file (points to the file selection icon next to the SVF File text box)
- The contents of the .svf display in the console (points to the main text area of the console)
- Status messages (points to the bottom status bar)
- Stop the player (points to the Stop button)
- Step through the JTAG commands (points to the Step button)
- Play the .svf (points to the Play button)

Notes

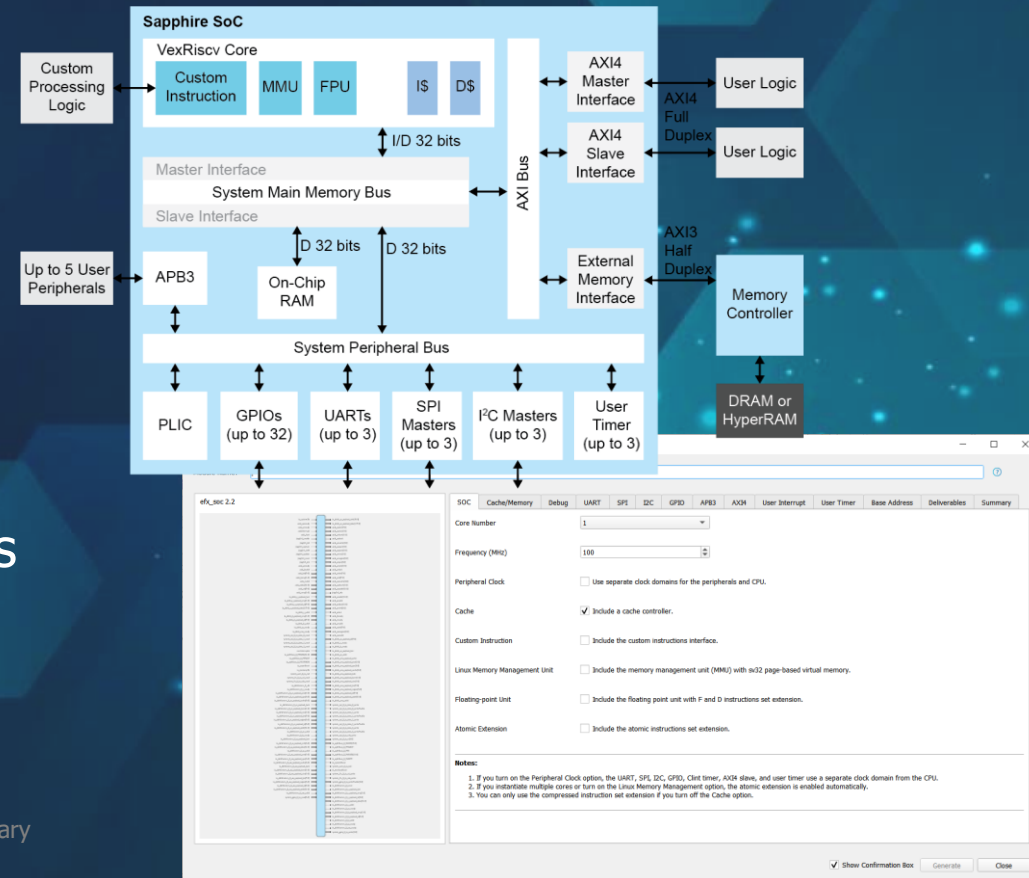
- With AES encryption enabled it is possible to use unencrypted bitstreams
- With RSA authentication only signed bitstreams are accepted
- Detailed description and examples can be found in [Efinity UserGuide](#)



SoftIP/ RISC-V[®] SOC offering

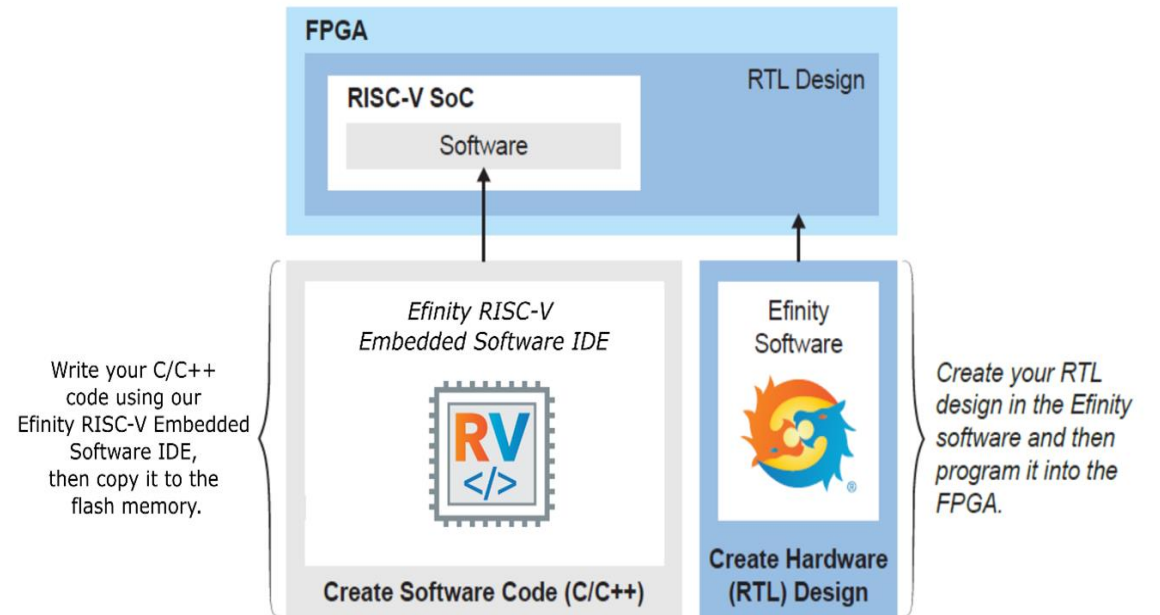
RISC-V Cores Implementation

- 65+ available now with commercial and open-source licenses
- Efinix solution based on VexRiscv by Charles Papon
 - 32-bit single core CPU
 - 6 pipeline stages
 - ISA RISC-V32I with extensions M, A, F, D
 - Includes a floating point unit
 - Includes an optional Linux memory management unit
 - Includes a custom instruction interface with 1,024 IDs to perform different functions
 - Supports optional RISC-V extensions such as atomic and compressed



Required Software and Tools

- Efinity[®] software
- Pre-compiled, open-source SDK
- Eclipse IDE for managing projects and software with Ashling GUI
- RISC-V GCC compiler and GDB debugger
- OpenOCD debugger for debugging applications
- Windows build tools (Windows)
- Available from our web page
 - <https://www.efinixinc.com/products-riscv.html>

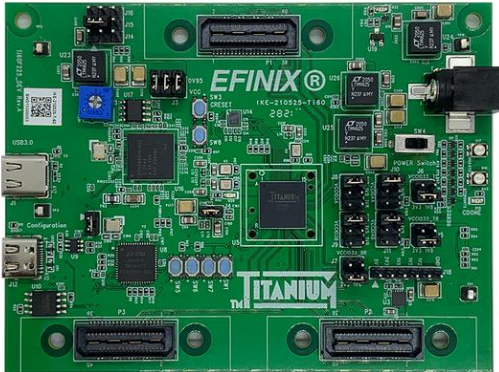




Development Kits

Development Kits

Titanium Ti60 F225 Development Board



Titanium Ti180 J484 Development Board



Trion T120 BGA576 Development Kit



Featuring T120 FPGA with hardened MIPI CSI-2 and DDR DRAM

Trion T120 BGA324 Development Kit



Featuring T120 FPGA with hardened MIPI CSI-2 and DDR DRAM

Trion T20 MIPI Development Kit



Featuring T20 FPGA with hardened MIPI CSI-2 and D-PHY

Trion T20 BGA256 Development Kit



Featuring the T20 BGA256 FPGA

Trion T8 BGA81 Development Kit



Featuring the T8 BGA81 FPGA

Xyloni Development Kit



Thumb-sized USB board for hobbyists and makers



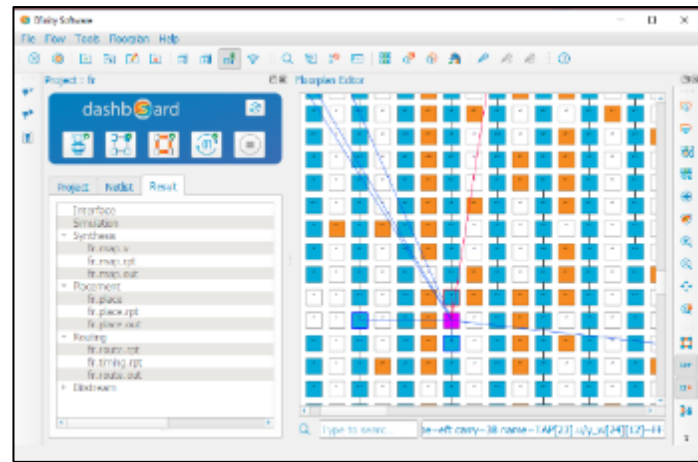
Software Efinity

Efinity[®] Integrated Development Suite

- Standard RTL-to-bitstream FPGA development tool (free of charge)
- Core and interface concept enables system integration

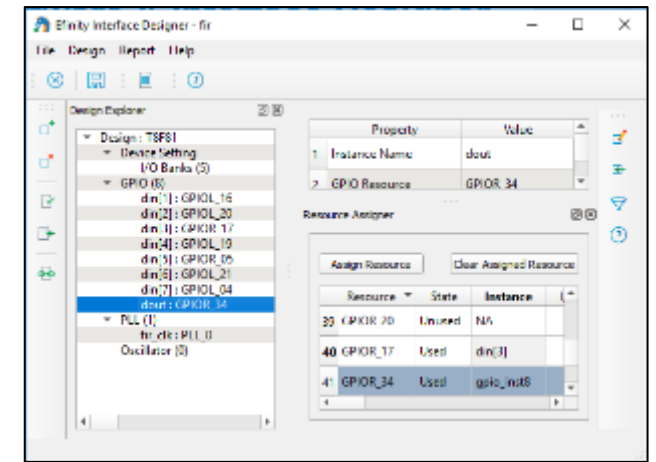
Core Designer

FPGA Core Fabric
(Synthesis, Place and Route)



Interface Designer

Subsystems
(I/O, DDR, MIPI, etc.)



Efinity[®] Integrated Development Suite

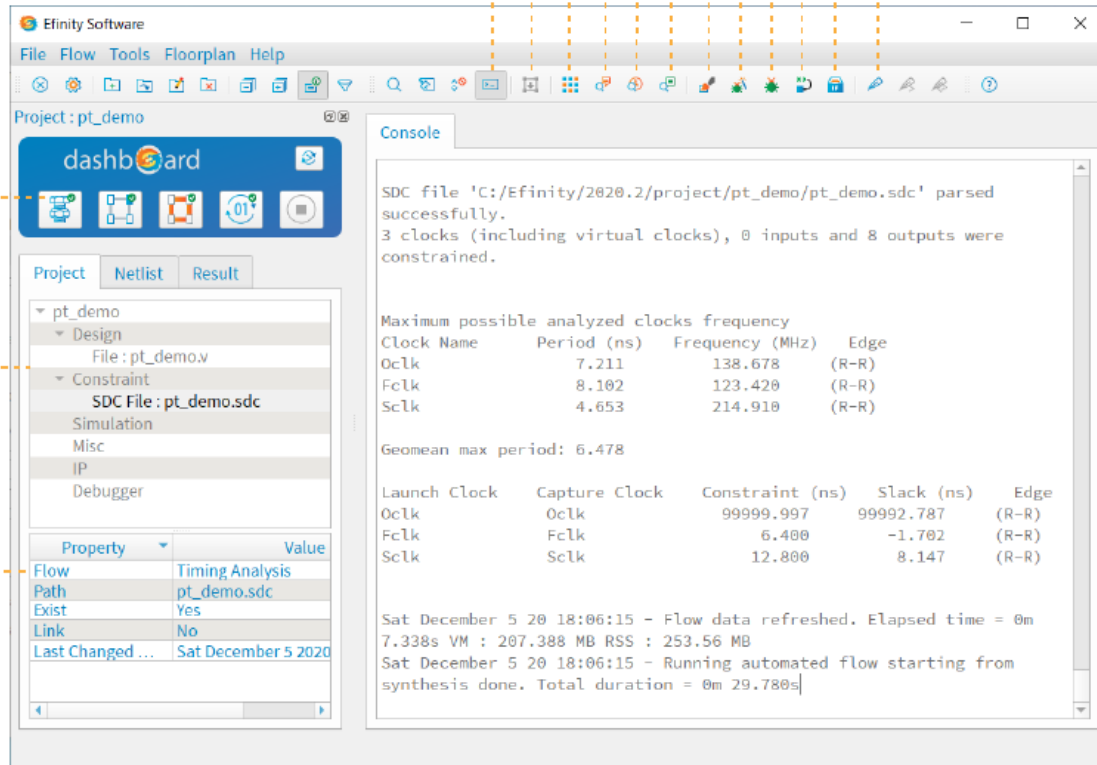
Main Window

- Log Browser
- Timing Browser
- Message Browser
- Floorplan Editor
- Load Place and Route Data
- Log Browser
- Interface Designer
- Debug Wizard
- Debugger
- Programmer
- IP Manager
- Tcl Console

Control the Software Flow

View Project Information

View Project Properties



Dashboard Control

- Toggle Automated/Manual Flow
- Start Synthesis
- Start Placement
- Start Routing
- Generate Bitstream
- Stop Flow

IP Catalog (2023.2)

The image displays two windows from the IP Catalog software. The left window, titled "IP Catalog", shows a search bar and a tree view of installed IP blocks under the "Efinix" category. The right window, titled "IP Configuration", shows the configuration for the "efx_soc 2.2.4" module. The configuration is organized into tabs: SOC, Cache/Memory, Debug, UART, SPI, I2C, GPIO, APB3, AXI4, User Interrupt, User Timer, Base Address, Deliverables, and Summary. The "SOC" tab is active, showing a list of IP blocks on the left and configuration options on the right. The configuration options include Core Number (set to 1), Frequency (MHz) (set to 100), Peripheral Clock (checkbox for separate clock domains), Cache (checkbox checked for include a cache controller), Custom Instruction (checkbox for include the custom instructions interface), Linux Memory Management Unit (checkbox for include the memory management unit), Floating-point Unit (checkbox for include the floating point unit), Atomic Extension (checkbox for include the atomic instructions set extension), and Compressed Extension (checkbox for include the compressed instructions set extension). A "Notes" section at the bottom provides additional information. At the bottom right of the configuration window, there are buttons for "Show Confirmation Box", "Generate", and "Close".

IP Catalog

Search

Installed IP

- Efinix
 - AXI Infrastructures
 - AXI Data FIFO
 - AXI Interconnect
 - AXI4-Stream Switch
 - Arithmetic
 - CORDIC
 - Divider
 - Integer Square Root
 - Bridges and Adaptors
 - APB3 to AXI4 Lite converter
 - Direct Memory Access
 - Ethernet
 - Triple Speed Ethernet MAC
 - MIPI
 - MIPI 2.5G CSI-2 RX Controller
 - MIPI 2.5G CSI-2 TX Controller
 - MIPI BIDIR DPHY RX
 - MIPI BIDIR DPHY TX
 - MIPI CSI-2 RX Controller
 - MIPI CSI-2 TX Controller
 - MIPI DPHY RX
 - MIPI DPHY TX
 - MIPI DSI TX Controller
 - Memory
 - BRAM WRAPPER
 - FIFO
 - Memory Controllers
 - ASMI SPI Flash Controller
 - DDR Hard Memory Controller - Calibration and Reset
 - DDR Hard Memory Controller-Reset
 - DDR3 Soft Controller
 - HyperRAM Controller
 - JTAG SPI Flash Loader
 - SD Host Controller
 - SDRAM Controller
 - Processors and Peripherals
 - Hard SoC
 - Sapphire SoC
 - Serial Interface Protocols
 - I2C
 - UART

IP Configuration

Module Name: test_name

efx_soc 2.2.4

SOC

Cache/Memory	Debug	UART	SPI	I2C	GPIO	APB3	AXI4	User Interrupt	User Timer	Base Address	Deliverables	Summary
Core Number		1										
Frequency (MHz)		100										
Peripheral Clock		<input type="checkbox"/>										
Cache		<input checked="" type="checkbox"/>										
Custom Instruction		<input type="checkbox"/>										
Linux Memory Management Unit		<input type="checkbox"/>										
Floating-point Unit		<input type="checkbox"/>										
Atomic Extension		<input type="checkbox"/>										
Compressed Extension		<input type="checkbox"/>										

Notes:

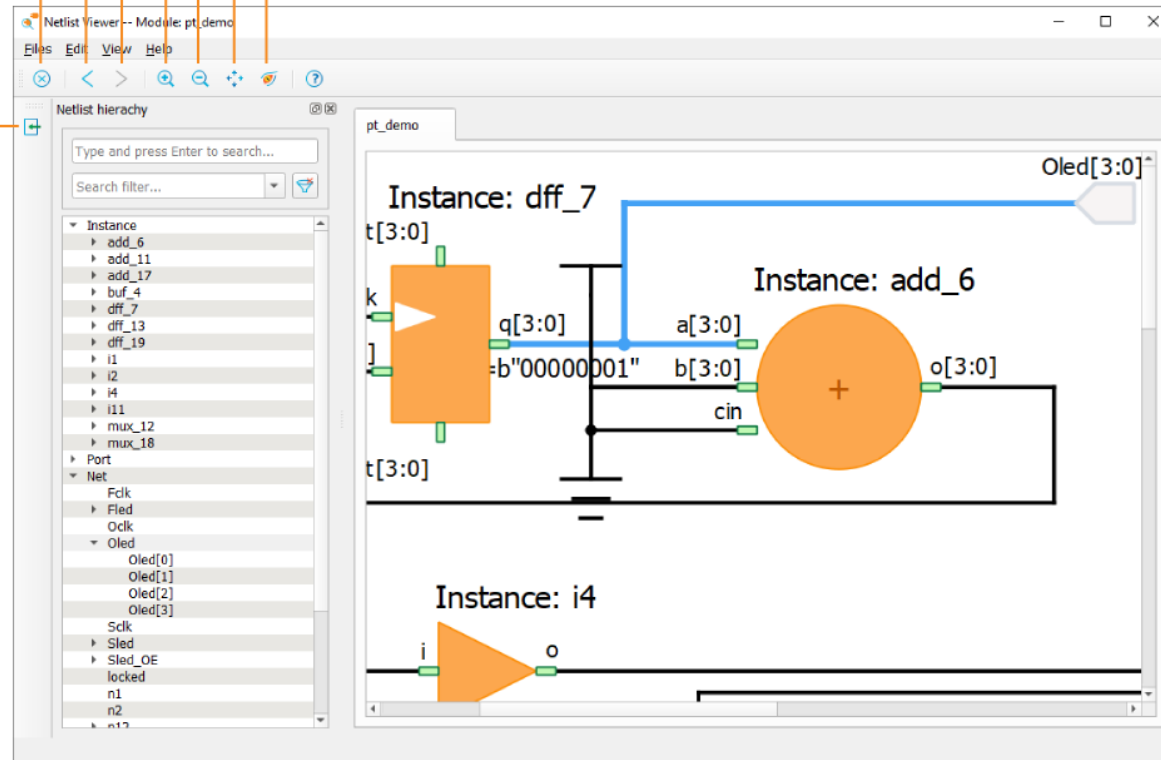
- If you turn on the **Peripheral Clock** option, the UART, SPI, I2C, GPIO, Clint timer, AXI4 slave, and user timer use a separate clock domain from the CPU.
- If you instantiate **multiple cores** or turn on the **Linux Memory Management** option, the atomic extension is enabled automatically.

Show Confirmation Box Generate Close

Configure and generate your specific IP Core/Module

RTL/Netlist View (2023.1)

- Show/hide Netlist Hierarchy pane
- Close
- Go to the previous action
- Go to the next action
- Zoom in
- Zoom out
- Fit the whole schematic in the viewer pane
- World view



Interface Designer

The screenshot shows the Efinix Interface Designer software interface. The interface is divided into several panels:

- Design Explorer (1):** A tree view on the left showing the project structure. It includes sections for Device Setting, I/O Banks (14), Configuration, GPIO (1), PLL (1), and various peripheral blocks like LVDS TX (0), MIPI TX (0), JTAG User Tap (0), and DDR (0). A search bar is at the top.
- Block Summary (2):** A table showing properties and values for the selected block. The table has two columns: Property and Value.
- Block Editor (3):** A form on the right for configuring the selected block. It includes fields for Instance Name, Mode, I/O Standard, Input Pin Name, Connection Type, Register Option, Double Data I/O Option, and Clock Pin Name.
- Design Explorer (6):** A vertical toolbar on the far left with icons for showing/hiding the Resource Assigner, adding/deleting blocks, and expanding/collapsing folders.
- Design Explorer (7):** A vertical toolbar on the far left with icons for adding and deleting blocks.
- Design Explorer (8):** A vertical toolbar on the far left with icons for expanding and collapsing the Design Explorer folder.
- Design Explorer (9):** A vertical toolbar on the far left with an icon representing the number of used blocks.
- File Design (4):** The top menu bar.
- Project Management Tools (5):** A toolbar at the top with icons for project management.

Property	Value
1 Instance Name	gpio_inst1
2 GPIO Resource	GPIOR_186
3 Mode	input
4 I/O Standard	3.3V LVTTTL / LVCMOS
5 Unused State	NA
6 Alternate Connection	PLL_CLKIN
7 Features	DDIO
8 Clock Region	R0
9 I/O Bank	3D_TR_BR
10 Pad	GPIOR_186_PLLIN0
11 Package Pin	U8
12 Input	
13 Pin Name	gpio_inst1
14 Connection Type	pll_clkln
15 Double Data I/O Option	none
16 Pull Option	none
17 Enable Schmitt Trigger	false

1. The Design Explorer shows the interfaces in your Design
2. Block Summary shows settings for the selected Block
3. Block Editor add or change settings
4. Import/Export GPIO assignments
5. Project Management Tools for design check
6. Show/Hide Resource Assigner
7. Block Tools add/delete blocks
8. Expand/Collaps Design Explorer folder
9. Number of used blocks()

Efinity® Integrated Development Suite

Debugger

Efinity Debugger

Select the correct USB JTAG device and click Connect Debugger to start debugging.

Run Run Immediate Stop

Core Status

Idle Waiting for Trigger Post-Trigger Full

Capture Status

Segment 0 of 1 Segment sample 0 of 1024 Total sample 0 of 1024

0% 0% 0%

Trigger Condition Global 'AND'

Name	Operator	Radix	Value	Port
state12:01	==	Bin	010	probe12:01

Program Console

Configuration

USB Target Trion T20MIPI Development Board

USB Info Bus 000 Device 255: ID 0403:6010

Bitstream tion/outflow/traffic_light.hex 20F169

Debugging 0x00210a79 USER1

```
Mon April 13 20 13:21:02 - pyftdi URL: ftdi://0x0403:0x6010:FT3KNTVS/2
Mon April 13 20 13:21:21 - JTAG (url=ftdi://0x0403:0x6010:FT3KNTVS/2) already in use! Try stopping debuggers before programming. Skipping...
```

GTKWave - C:\Efinity\Projects\traffic_light_GOLDEN_manual-insertion\traffic_light_GOLDEN_manual-insertion\la0_waveform.vcd

File Edit Search Time Markers View Help

From: 0 sec To: 10230 ns Marker: 49 ns Cursor: 40 ns

SST

Signals

Time

led[2:0]=4

state[2:0]=1

count[25:0]=2

Waves

ns 40 ns 56 ns

4

1

2FAEE85 2FAEE86

Type Signals

Filter:

Append Insert Replace

ISO26262/ ICE61508



The manufacturer may use the mark:



Revision 1.0 August 4, 2023
Surveillance Audit Due
September 1, 2026

Certificate / Certificat Zertifikat / 合格証

EFI 2207092 C001

exida hereby confirms that the:

Efinity® IDE and Toolchain v2023.1

**Efinix Technology (M) Sdn. Bhd.
Penang - Malaysia**

Has been assessed per the relevant requirements of:
IEC 61508:2010 and ISO 26262:2018

and meets requirements providing a level of integrity to:
SIL 4 / ASIL D Qualified

Tool Functions:

The Efinity® IDE and Toolchain suite is an integrated development environment designed for Efinix FPGA development. Using Efinity, customers can develop, compile and test their FPGA design from RTL source code all the way down to bitstream programming on FPGA development boards.

Application Restrictions:

The tools of the Efinity® IDE and Toolchain must be used per the defined use cases, and all requirements specified for the tool users (conditions and assumptions of use) shall be fulfilled, as described in the Functional Safety Manual for each tool.

Efinity® IDE and
Toolchain

Certificate / Certificat / Zertifikat / 合格証

EFI 2207092 C001

SIL 4 / ASIL D Tool Qualification:

The Efinity® IDE and Toolchain have met the requirements for support tools up to Safety Integrity Level (SIL) 4 of IEC 61508-3 (section 7.4.4). The product has also met the requirements for confidence in use of software tools of Automotive Safety Integrity Level (ASIL) D of ISO 26262-8 (Section 11). These are intended to achieve sufficient integrity against systematic errors of design by the manufacturer.

Tool Confidence Level (TCL)

Several use cases were defined for each Efinity® IDE tool. A software tool evaluation according to ISO 26262-8, clause 11 determined a required tool confidence level of TCL1 for all tools and use cases, without the need for software tool qualification. Individual tools or the complete tool chain can be used in the development of FPGAs with allocated safety requirements up to ASIL D.

Tool users must confirm the validity of the pre-determined TCL1 in their own design environment, and confirm that all tools are used per the defined use cases and that all conditions and assumptions of use (CoU and AoU) are fulfilled, as specified in the tool functional safety manuals. Otherwise, tool users must perform their own detailed software tool evaluation and possibly software tool qualification.

The following documents are a mandatory part of the certification:

exida Assessment Report:

- EFI 22-07-092 R011 V1R1 61508 26262 Tool Assessment Report - Efinix IDE

Efinix Functional Safety Manuals:

- Efinity_IDE Functional Safety Manual v3 or later
- Interface_Designer Functional Safety Manual v2 or later
- IP_Manager Functional Safety Manual v2 or later
- Code_Editor Functional Safety Manual v2 or later
- Synthesis Functional Safety Manual v2 or later
- PhR Functional Safety Manual v2 or later
- Bitgen Functional Safety Manual v2 or later
- Programmer Functional Safety Manual v2 or later
- Timing_Engine Functional Safety Manual v2 or later
- Debugger Functional Safety Manual v2 or later



Efinity Features

- Project management to keep your design files organized
 - Support for Verilog HDL , System Verilog and VHDL languages
 - Graphical views of design hierarchy, result files, and reports
- VHDL LIBRARY support
- Easy to use dashboard to run through the flow (synthesis, placement, routing, bitstream generation) automatically or manually
- IP Manager to configure IP cores
- Support for Python scripting and command line tool flow
- Interface Designer to constrain logic and assign pins to blocks in the device periphery
- Floorplan Editor to browse through your design's logic and routing placement
- Timing Browser and static timing analysis to measure your design's performance
 - Tcl Command Console to perform timing analysis
- Supports simulation flows using the ModelSim, Aldec, NCSim, or free iVerilog simulators
- GUI and command-line Programmer
- Efinity Debugger with Virtual I/O and Logic Analyzer debug cores



System Needs

Product	Model	Memory
Trion	T4, T8, T13, T20, T35	16 GB
	T55, T85, T120	32 GB
Titanium	Ti35, Ti60	16 GB
	Ti90, Ti120, Ti180	32 GB

- Minimum requirements
 - Computer with a 64 bit operating system, dual-core processor, and 16 GB RAM
- Linux environments
 - Operating system: Ubuntu x86-64 v18.04 or later, Red Hat Enterprise x86-64 v7.4 or later
 - Linux X11 windowing system (for Efinity® GUI)
 - Udev device manager for Efinix USB programming cable
 - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: <https://developers.redhat.com/products/openjdk/download> (OpenJDK 8 or 11) – <http://jdk.java.net/16/> (OpenJDK 16)
- Windows environments
 - Windows 10 or later, 64 bit
 - Microsoft Visual C++ 2019 x64 runtime library (or latest version)
 - Open-source Java 64-bit runtime environment; required for configuring the Sapphire RISC-V SoC in the IP Manager; available from: – <https://www.java.com/en/download/manual.jsp> (Java 8)

Contact Data EMEA

Harald Werner

Efinix GmbH

EMEA Senior Sales Director
and General Manager

Phone: +49 171 696 2330

E-Mail:

haraldw@efinixinc.com

Joachim Mueller

Efinix GmbH

FAE Manager EMEA

Phone: +49 171 696 2331

E-Mail:

joachimm@efinixinc.com

Contact Data EMEA

Maximilian Werner

Efinix GmbH

FAE EMEA

Phone: +49 171 696 2332

E-Mail:

maximilianw@efinixinc.com

Fabian Heinrici

Efinix GmbH

RSM EMEA

Phone: +49 171 696 2333

E-Mail: fabianh@efinixinc.com

Web Registration

- For support page access
<https://efinixinc.com/support/account.php?do=create>



Thanks !